LTPS-TFT Process for OLED and some issues generated from the manufacturing†

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Abstract

AMOLED (Active-matrix organic light emitting diode) is a new display technology used in flat panel display which has wider color gamut, higher contrast ratio, lower consumption than LCD and can achieve flexible display. However, LTPS (Low Temperature Poly-Silicon)-TFT (Thin Film Transistor), is now a highlight of Active Matrix Driving. As a current source, in order to drive it, there needs more TFTs and higher driven current for OLED. Compared with the traditional a-Si TFT, LTPS-TFT possesses the high mobility (≈100 cm²/V • s) and low off current poly-silicon's character which is known as being high resolution ratio, quick reacting, wide aperture ratio and high integration. In this paper, we will discuss the common process of LTPS which is made in a relatively low temperature condition. Then we will talk about some display issues caused by LTPS process, such as mura, hysteresis and light spot, e.t.

Author Keywords

AMOLED, LTPS-TFT, mura, hysteresis, light spot

1. Introduction

1) Compared with mainstream technology LCD at present, OLED technology has its innate advantage such as better viewing result, thicker, lower energy consumption and being able to achieve flexible display [1]. As the mass productive technology is becoming mature, disadvantages which blocks its developing way have been solved one by one. And its merits are being highlight which result in rapid improvement of demand. According to some prediction, Chinese OLED market requirement in 2018 would reach to 240 million pieces. And in the coming 5 years (2018-2022), compound growth rate would be about 18.17% every year, when finally 468 million pieces display panel might be demand [2].

2) Although demand is growing every year, the manufacturing process of AMOLED differs from AMLCD. Several aspects are as below:

Circuit Design: OLED is a kind of current source device. So its pixel circuit consist of two TFTs and one capacity at least. One of its TFT is used as driver TFT which control the current flow through it from the power supply side(VDD). While AMLCD, however, need only one TFT and capacity to drive. The simplest pixel circuit designs of AMOLED and AMLCD can be seen as figure 1.

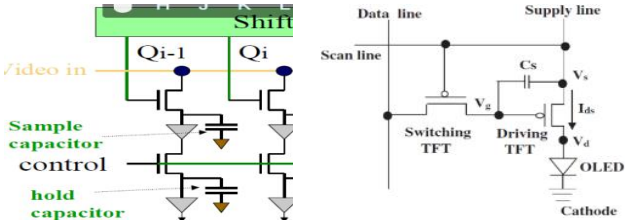

Figure 1. LCD (left) and AMOLED pixel circuit (right)

TFT Structure: While LCD must let light go through itself from back light, AMOLED can let emission light emit toward only one direction. So AMOLED normally use top-emission structure, and there is no need to make shield for channel, which is semiconductor. On the other hand, AMOLED uses P type Silicon instead of N type because N type Silicon has the hot carrier effect and P type Si may have a better performance when voltage inverses for driving. What's more, pixel definition layer, spacer and planarization layer are needed in TFT structure of AMOLED.

3) On account of many differences between AMOLED and AMLCD, the LTPS-TFT process are not complete the same. And the failure mechanism of AMOLED is also worth to discuss. In this article, we will discuss the process of AMOLED first. And then we may try to explore some simple and common issues of AMOLED display panel generated from LTPS process.

2. AMOLED's TFT process

2.1.Structure and Solution: As the manufacturing technology develops, many kinds of LTPS solution has been come out. And mask number become less and less-10, 8, 5 mask solution. However, here we are going to discuss a common solution which uses 8 mask, P type Silicon, top gate and emission structure. The main arrangement of mask can be seen below(figure 2):

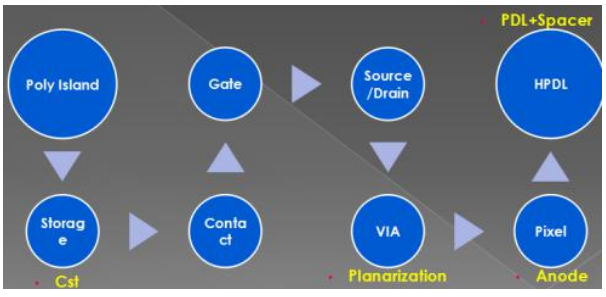

Figure 2. Arrangement of 8 mask top-gate TFT process

2.2.Main process of LTPS-TFT: 8 mask top-gate TFT with

P type silicon:

Mask 1: poly-silicon island builds up from a-Si (figure 3).

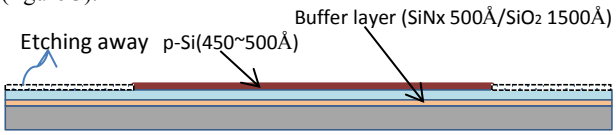

Figure 3. Active layer patterning

- a-Si + buffer film deposition using PECVD:

The a-Si layer(450-500Å) is amorphous silicon which is going to be crystallized into poly-silicon as semiconductor and so called channel, poly-silicon island, active layer or PSI.

The SiN_x layer(500Å) possess the function that block the impurities away from glass such as Na^+, Ca^+ and Mg^+ etc.

The SiO_2 layer(1500Å) can be well infiltrated with a-Si, so that deposited a-Si has fewer defect and good quality. What's more, it is said that SiO_2 can slow down the temperature diffusion which is good for formation of big poly-Si grain in ELA process.

- Dehydrogenation with furnace:

a-Si film contains a certain amount of H, which may cause H explosion in ELA program. For the above reason, deposited a-Si film must be annealed at high temperature (500℃).

- ELA:

Excimer Laser Anneal uses laser energy to make a-Si melt and then liquid Si will change into poly-Si due to the dynamic growth for crystallization.

- Poly-Si Photo, Dry Etching, and Stripper. (classical semiconductor process for film circuit and pattern, which is Mask 1)

Mask 2: Storage pattern with Gate insulator and channel doping. (figure 4).

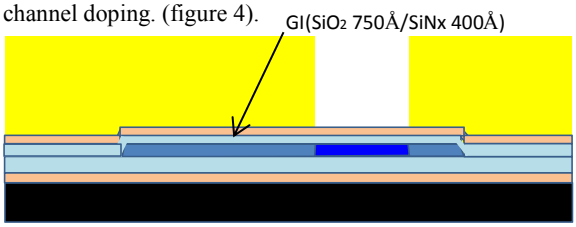

Figure 4. Storage patterning

- Channel Doping. To control the absolute value of V_{th} under a certain value for voltage driving, we here do weak B^+ or P^+ doping by implantation.
- Gate Insulator, which is crucial in TFT structure, can be made by PECVD. However, the reason why we usually use SiN_x(400Å) + SiO_2(750Å) as GI may be that when SiN_x and SiO_2 combine together, the breakdown voltage of GI might be larger than single of them.
- Storage Photo. As the p-Si in the storage area will be blocked by Gate pattern. We here need a mask to block non-storage area from doping ions. And then poly-silicon's storage pattern will be formed.
- Storage Doping. Only when we change the resistance of p-Si into conductive can we take p-Si as a part of capacity (bottom electrode/pole), which is to ensure that storage's bottom electrode part have a high conductivity to storage charges.
- PR (Photo Resist) stripping. PR is not what we want.

Mask 3: Gate pattern with S/D(Source/Drain) doping. (figure 5)

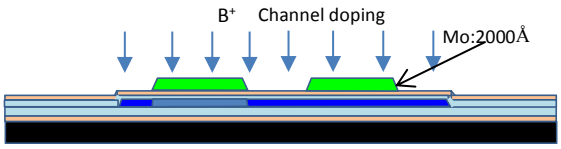

Figure 5. Gate patterning

- Mo film(2000Å) made by Sputter.
- Gate Photo, Dry etching and Stripping. However, the precision of Gate pattern and the taper control in photo and dry etching are most important in this part.
- S/D Doping. Except for channel section of poly-Silicon island, there is also S/D portion, which requires high conductivity so that it is able to form ohmic contact with S/D metal layers. Hence, strong dose of B^+ doping is needed in this process.

Mask 4: Contact Photo with ILD films and activation. (figure 6)

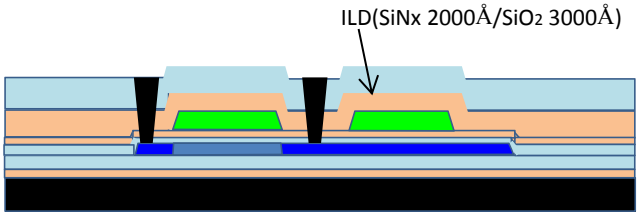

Figure 6. Contact hole patterning

- ILD = SiN_x(2000Å) +SiO_2(3000Å).

Inter Layer Dielectric(ILD) are built for dielectric between Gate and S/D metal layers and can protect TFT from pollution. However, high H-content SiN_x film enables the function to be the H-supplement for poly-silicon's dangling bond, where defects may occur.

- Contact Hole Photo, Dry etching and Stripping. To make contact between S/D metal, S/D p-Si and some other connection especially peripheral patterns, contact holes is needed where taper angle and etching residual is a big challenge.
- Wet Etching. Wet etch has high selection ratio

between poly-Si and the above PECVD's films for fewer residual in the hole.

Mask 5: S/D Photo with metal anneal. (figure 7).

- Ti/Al/Ti(1000Å/4000Å/800Å) metal films make by sputter. It is said that Ti films enable the function of protecting Al film from oxidation and generating hillocks. And it can also protect p-Si from Al's contamination.
- Source and Drain Photo. Metal lines which connect metal lines on other layer and usually act as data transmission and large power transmission role.
- Metal Anneal. Anneal for better connection between p-Si and S/D and better uniformity of V_{th}.

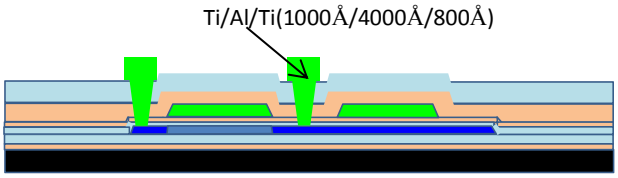

Figure 7. Source/drain patterning

Mask 6: VIA Photo. When planarization is needed for fewer short and open issues of OLED material on account of sags and crests caused by under layers, a hole via planarization layer has to be built to make connection for anode layer. However, there is no need for etching process while planarization film is made of PI material (PI Coating Film) and it can be developed a hole. (figure 8).

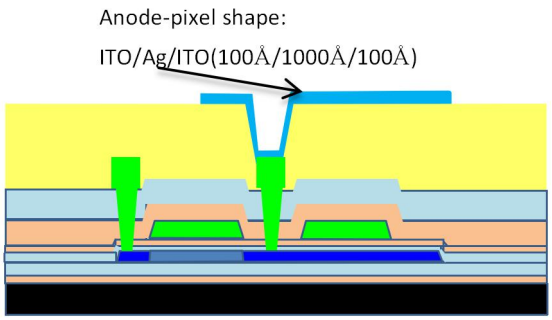

Figure 8. Via hole and anode patterning

Mask 7: Anode Photo makes the shape of pixel. (figure 9).

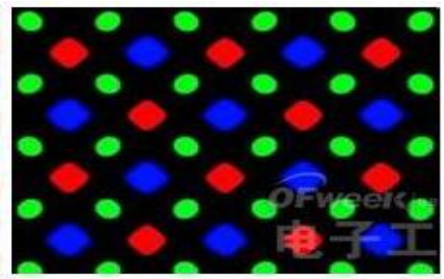

Figure 9. Shape of pixel (Anode patterning)

- Anode films make by sputter. The reason of structure ITO/Ag/ITO(100Å/1000Å/100Å) is that firstly, Ag has a high reflecting rate of vision light so that it can reflect the light emitted from OLED device, which is a crucial part of top emission structure. Secondly, ITO films can protect Ag from oxidation and the top layer which is going to contact with OLED layer possesses a matched work function with OLED material.
- Anode Photo, Wet Etching and Stripping. Do photo process for pixel patterning which has different sizes and different shapes.

Mask 8: HPDL Photo. In this part, PDL (Pixel definition Layer) and Spacer layer can be made in one process using Half-Tone Exposure. This is a technology that can make different pattern in one photo process by using absolute transmissible mask and half transmissible mask. When light penetrates through half transmissible mask, it can be a different pattern in a different altitude. (figure 10)

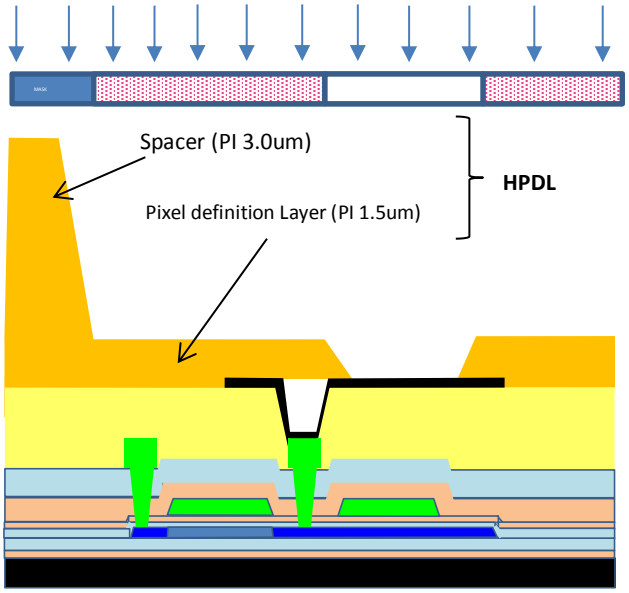

Figure 10. HPDL process using half-tone exposure

- PDL is a kind of defining the region of pixel or where OLED material should be evaporated. And it can also be fewer the short and open issues happened in OLED device by making good taper instead of bad taper angle in anode pattern.
- Spacer layer is similar to spacer of LCD. It can support the pressure from encapsulation and protect

device under it. However, it's height is also affecting the evaporation process.

3. Some issues generated from LTPS:

The non-uniformity of the display image is a serious problem since the luminance of pixels is very sensitive to the variation of the LTPS-TFT characteristics in the conventional pixel structure that consists of two transistors and one capacitor. [3] So process of LTPS can causes many problems.

3.1.Mura Issue:

3.1.1.PIN/PAD Mura (figure 11):

Figure 11. PIN/PAD mura

- **Defect definition :** When panel displays as a normal or gray image, there are some circle or spot area which is brighter or darker than nearby area.
- **Essential reasons:**

  We believe that this kind of Mura is caused by:

  1. **Temperature** differs from normal area when processing, especially some thermal process. However, p-Si is a sensitive part of LTPS-TFT. Hence, a little thermal difference can make diversity between TFT and TFT, including a-Si process in PECVD.

  2. **ESD damage** which can cause TFT's character shift such as V_{th}, SS and mobility.

- **How to solve:**

  1. Find better parts for equipment with suitable material.

  2. 'AA'(Active Area) design pattern evades PIN area.

3.1.2.ELA Mura - shot and scan mura: (figure 12)

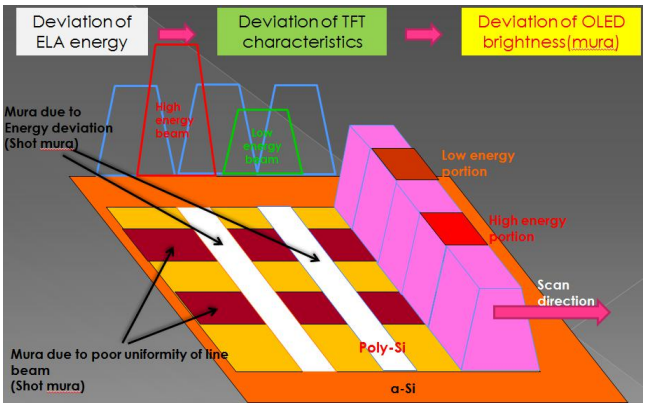

Figure 12. Shot and scan Mura

- ELA process causes serious OLED mura due to pulse energy deviation and poor uniformity of laser line beam, which is so called shot and scan mura. The mechanism to form mura may be: deviation of ELA energy causes deviation of TFT characteristics. Then deviation of OLED brightness (mura) may occur due to deviation of TFT characteristics.

3.1.3.ELA Mura - oblique mura:(figure 13)

- **Feature :**

  1. It is extremely regular among mura to mura, including space, inclining angle and strength;

  2. Mura performance is related to pixel design especially pixel size.

  3. Mura performance is related to ELA pitch value, and it is not a strictly linear relation.

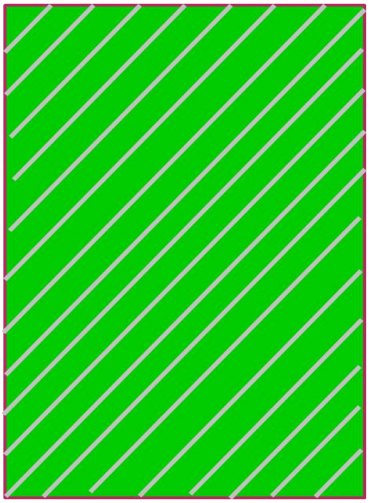

Figure 13. Oblique mura

- **Essential reasons :**

  We believe that I_{on} is related to the number of channel's boundaries in poly-Si, and if the channel periodically contains different number of boundaries, the OLED brightness may deviate periodically due to I_{on} deviation.

- **How to solve：**

  As can be seen in the above feature, design and ELA pitch is to be matched to solve this mura issue:

  1. Change the design of pixel size or ELA pitch, find the matching value so that no or less diffraction can form when displaying.

  2. Simulate the design and ELA material in software before trial-production.

3.1.4.Photo Mask and Design Mura: (figure 14)：

- **Simple Description：**

  When design precision is not match to photo mask's precision, it may come out some mura due to the deviation between design and process.

- **How to solve:**

  Match the precision between design and mask.

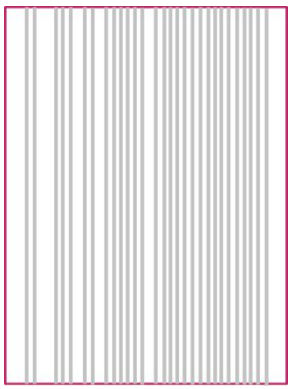

Figure 14 Photo mask mura

3.1.5.Cleaning Mura: (figure 15)：

- Simple Description：

  As we can see, p-Si is a sensitive part of TFT. Sometimes, deviation of cleaning process can also cause mura issues. For example, if the pressure and flow of water curtain too high or low, mura may appear.

  However, in GI or S/D's pretreatment process, we usually use DHF as cleaning material, and deviation of water curtain, air curtain and air knife may cause mura easier.

Figure 15. Cleaning mura

3.2.Light Spot:

3.2.1.Weak Light Spot : (figure 16)

- **Defect definition：**

  When Panel displays as a black image, some week monochromatic light spots can be seen in a relatively dark environment.

- **Feature：**

  1. There is no particle/pattern error below or above the light spot area;

  2. It's relatively weaker brightness than strong light spot;

  3. Most of it can be reduced by TFT aging.

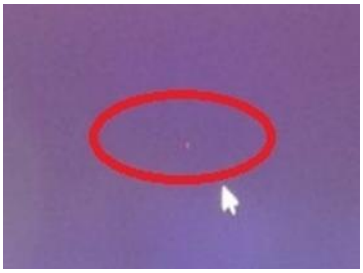

Figure 16. Weak light spot

- **Essential reasons：**

  We believe that this kind of weak light spot is caused by TFT's current leakage, which is big enough to light OLED device even though TFT is off.

- **How to solve:**

  TFT aging: load strong and long enough bias voltage on the TFT so that there may come out some charges to invalid the defects between GI and channel.

3.2.2.Strong Light Spot:(figure 17)

- **Defect definition:**

  When Panel displays as a black image, some strong or big light spots can be seen in a relatively dark environment.

Figure 17. Strong light spot

- **Feature：**

  1. There are pattern errors below the light spot area, where the pixel circuit is built, such as short and open. However, pattern errors are generated from particle issue mostly nowadays.

  2. Relatively stronger brightness than weak light spot;

  3. It can't be reduced by TFT aging.

- **Essential reasons：**

  As we can see from the below image, which is a simple OLED driving circuit. When data signal cannot be loaded or stored in the last frame, OLED device always emits abnormally. And when we use P type Si as channel material, Gate short with grounding or low level signal, T2 will always open, and then OLED will bright. However, short or open issues are mostly caused by particle issue which can make residual in the photo or etching process and can make patterns warp.

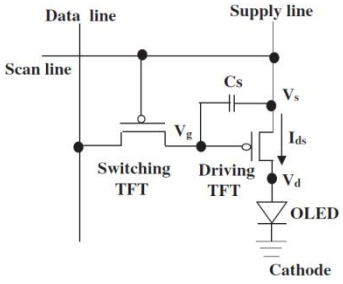

Figure 18. AMOLED pixel circuit

- **How to solve：**

  Reduce particle, including particles from metal and insulator layer.

3.3.Hysteresis:

- **Hysteresis phenomenon:**

  As is shown in the figure 19 (the I_{ds}-V_{gs} transfer characteristics forward gate voltage sweep and reverse gate voltage sweep in p-type poly-Si TFT), the difference in the threshold voltage(V_{th}) is indicated by the gate voltage sweep direction. The figure shows that the $|V_{th}|$ of reverse gate voltage sweep is larger than that of forward gate voltage sweep.

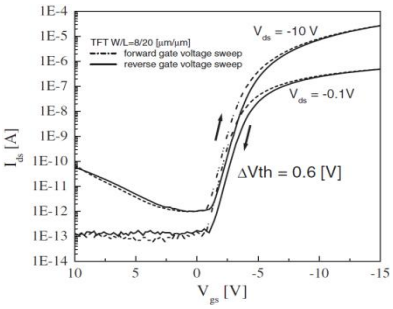

Figure 19. I_{ds}-V_{gs} transfer characteristics

- **Hysteresis affection and mechanism [4~5]:**

  Hysteresis can be explained by the effective interface charge: The hysteresis of p-type poly-Si TFT is induced by hole trapping in the oxide trap states and interface trap states between the poly-Si layer and gate insulator. Holes can be trapped and de-trapped repeatedly depending on the applied voltage. As hole trapping occurs at the negative starting gate voltage under a condition, the transfer characteristics exhibit a parallel shift toward the negative voltage. This causes, the $|V_{th}|$ to increase and the channel current to decrease in proportion to the quality of the trapped charge. For positive starting voltage in the forward gate voltage, the trapped charge should be de-trapped, which would cause the $|V_{th}|$ to decrease and the channel current increase.

- Take an example as figure 20, we simulate in the device through changing the display mode. White to Gray mode equals to reverse sweep while Black to Gray mode equals to forward sweep.

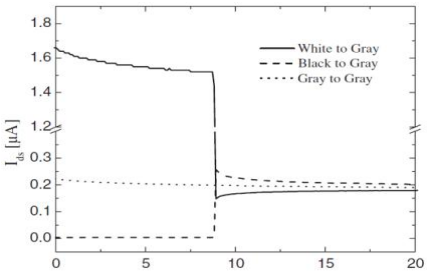

Figure 20. Simulation and test of hysteresis

- **When phenomenon above happened, residual image may occur. (Figure 21)**

Figure 21. Sticking phenomenon of OLED recession

- **Residual Image:**

  Generally Speaking, residual image is classified into two types.

  One is irrecoverable residual image which is caused by the degradation of the OLEDs or driving TFTs with emitting time.

  The other is the recoverable residual image, which is related to the hysteresis of driving TFTs.

- **How to solve** - improve the reliability of TFTs:

  1. Eliminate ESD issues;

  2. Test and improve the film quality of GI, taper angle of Gate and S/D;

  3. Evaluate a better method for GI pretreatment, including DHF cleaning and GI pre-plasma treatment [6] before main deposition step.

  4. Evaluate a fitter temperature of all high temp annealing, such as dehydrogenating annealing, metal annealing and activation annealing.

4. Conclusion

In this article, we have discussed the process of AMOLED first. And then we tried to explore some simple and common issues of AMOLED panel generated from LTPS process. Such as Mura, Light Spot and Hysteresis. However, there are many kinds of process program for LTPS and much more defects we haven't talked about, that remains a long topic to say.

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